KAKATIYA UNIVERSITY: WARANGAL
TIME TABLE M.TECH I Year I SEMESTER EXAMINATION

CENTRE: ***KU COLLEGE OF ENGINEERING & TECHNOLOGY, KU CAMPUS WARANGAL.***

a) Kakatiya Institute of Technology and Science, Warangal b) Warangal Institute of Technology & Science, Oorugonda, Warangal

c) Chaitanya Institute of Technology & Science, Kishanpura, HNK d) Vinuthna Institute of Technology & Science, Hasanparthy

e) KU College of Engineering & Technology, KU Campus

TIME:: 02.00 pm to 05.00 pm

Date & Day	Structural & Construction Engineering (6001)	Design Engineering (6301)	Digital Communication (6601)	Software Engineering (6901)	Computer Science and Engineering (7601)	VLSI & Embedded System Design (7201) and VLSI Systems Design (7401)	CAD/CAM (6401)	Power Electronics (7901)
16-05-2015 Saturday	Numerical and Statistical Methods	Optimization Methods in Engineering Design	Detection & Estimation Theory	Discrete Mathematics & Optimization Techniques	Data Structures and Algorithms Design	Optimization Techniques & Graph Theory (VLSI & Embedded System Design Only) Advanced Digital Signal Processing (VLSI Systems Design Only)	Optimization Methods in Engineering Design	Machine Modeling & Analysis
19-05-2015 Tuesday	Limit Analysis of Concrete Structures	Fundamental Principles of Engineering Design	Data & Computer Communication	Object Oriented Software Engineering	Advanced Software Engineering	Digital Design (Common VLSI & Embedded System Design and VLSI system Design)	Fundamental Principles of Engineering Design	Analysis of Power Electronic Converts
21-05-2015 Thursday	Advanced Concrete Technology	Stress Analysis	Advanced Digital Signal Processing	Software Project Management	Computer Networks and Security	Analog Design (Common VLSI & Embedded System Design and VLSI system Design)	Stress Analysis	Modern Control Theory
23-05-2015 Saturday	Advanced Analysis of Structures	Mechanical Vibrations	Microwave & Optical Fiber Communication System	Advanced Operating Systems	Data Mining & Data Warehousing	VLSI Technology (Common VLSI & Embedded System Design and VLSI system Design)	Mechanical Vibrations	Power Electronic Controls of DC Drives
25-05-2015 Monday	Construction Techniques and Equipment	Computer Aided Design & Graphics	Data Compression Techniques	Advanced Computer Architecture	Advanced Computer Architecture	Embedded Systems Concepts (Common VLSI & Embedded System Design and VLSI system Design)	Computer Aided Design & Graphics	Elective – I HVDC Transmissions
27-05-2015 Wednesday	**ELECTIVE – I** Total Quality Management	**ELECTIVE – I (d) Smart Structures** (DE Only)	**ELECTIVE – Embedded System Design Artificial Neural Network**	**ELECTIVE – I** (a) Data Structures & Algorithms (d) Genetic Algorithms	**Elective – I Advances in Compiler Construction**	**ELECTIVE – I** Data Communication & Computer Networks (Common VLSI & Embedded System Design and VLSI system Design)	**ELECTIVE – I (d)** a) Fault Diagnosis of Machines	Elective – II Alternative Sources of Electronic Energy

CONTROLLER OF EXAMINATIONS

Note: - *Any Omission or Clash in the Time-Table may kindly be intimated to the Controller of Examination, K.U., Warangal, immediately.*